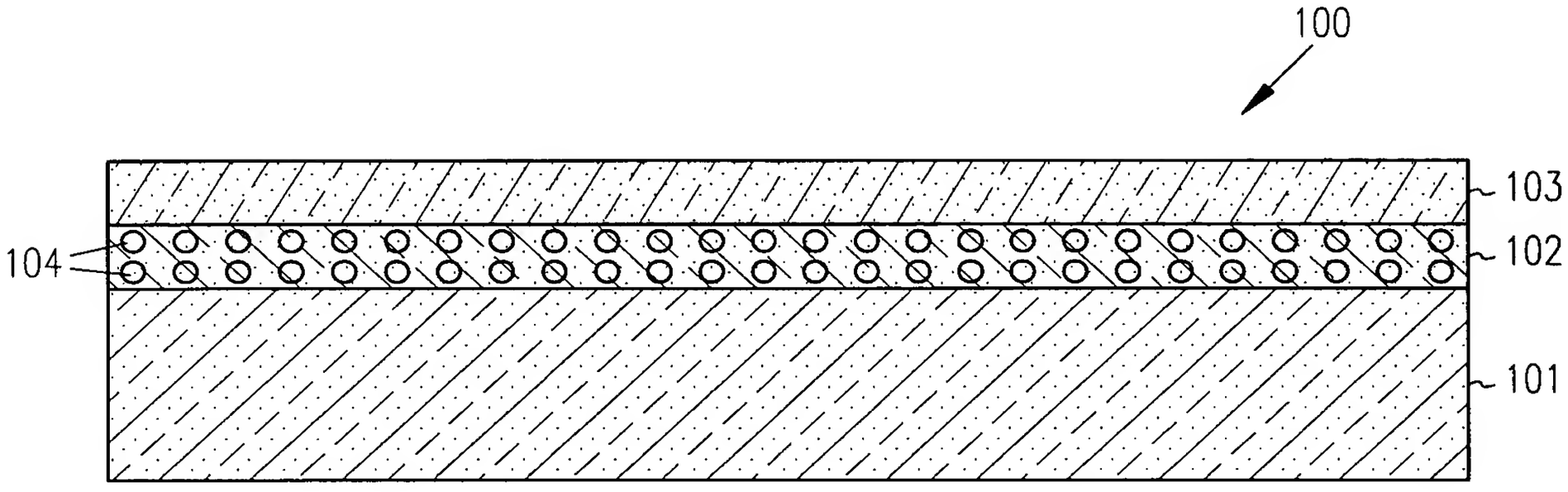

FIG. 1

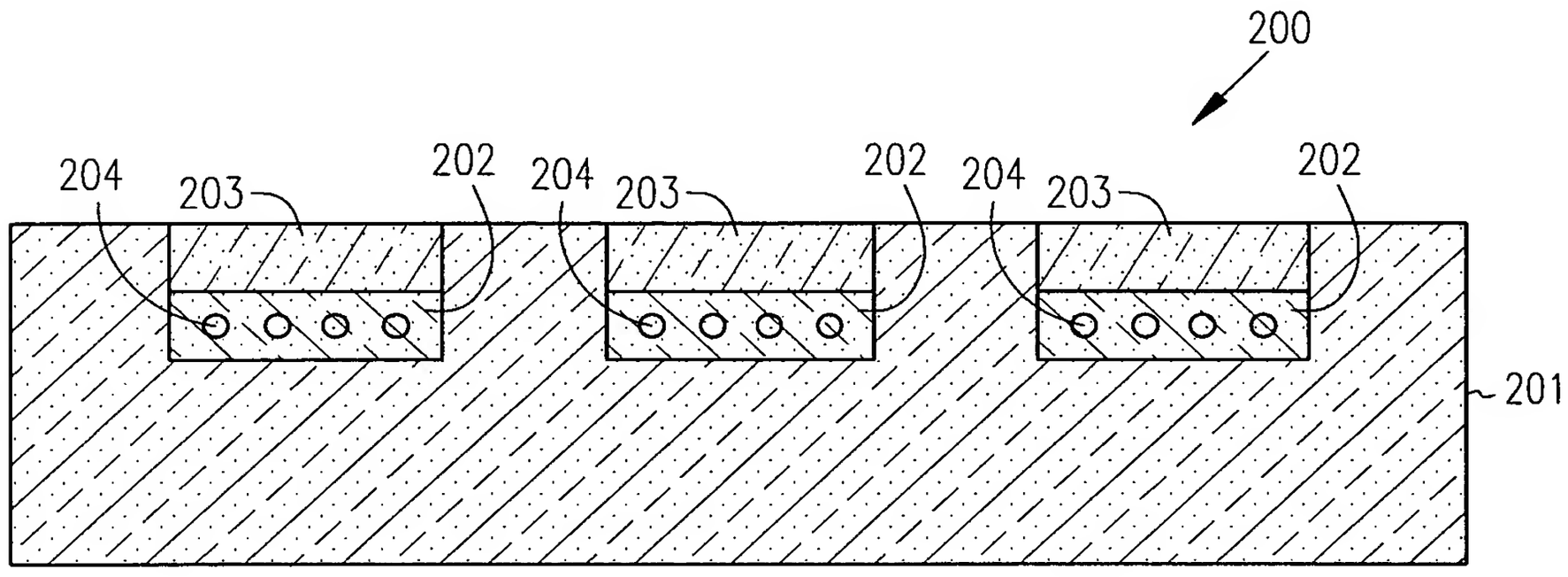

FIG. 2

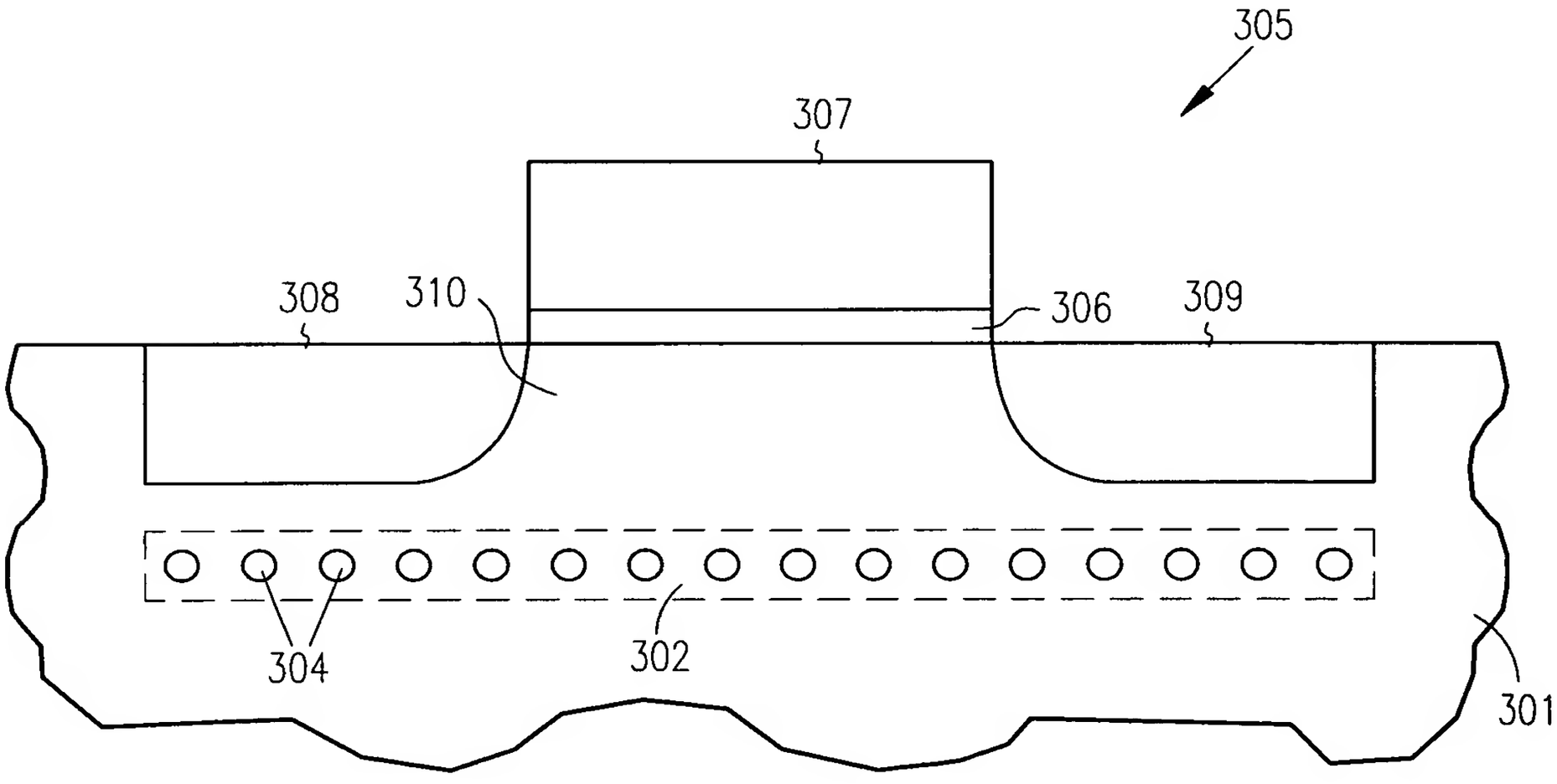

FIG. 3

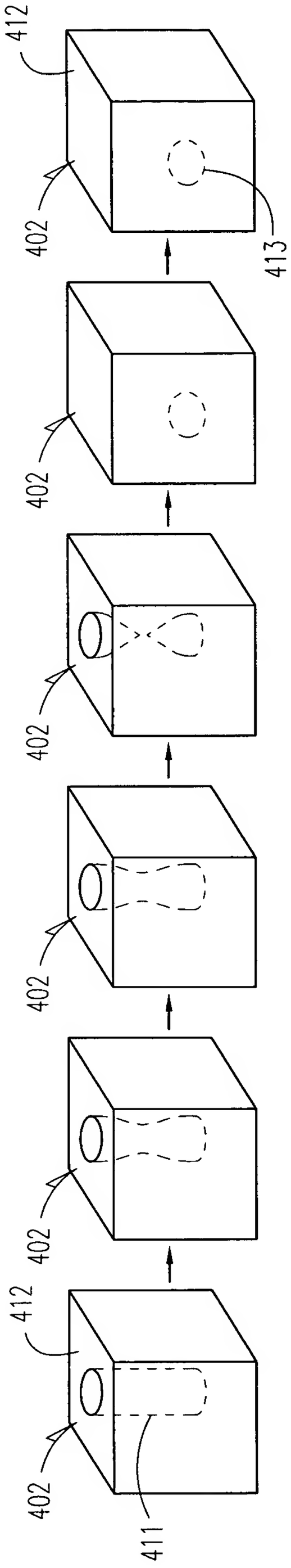

FIG. 4F FIG. 4E FIG. 4D FIG. 4C FIG. 4B FIG. 4A

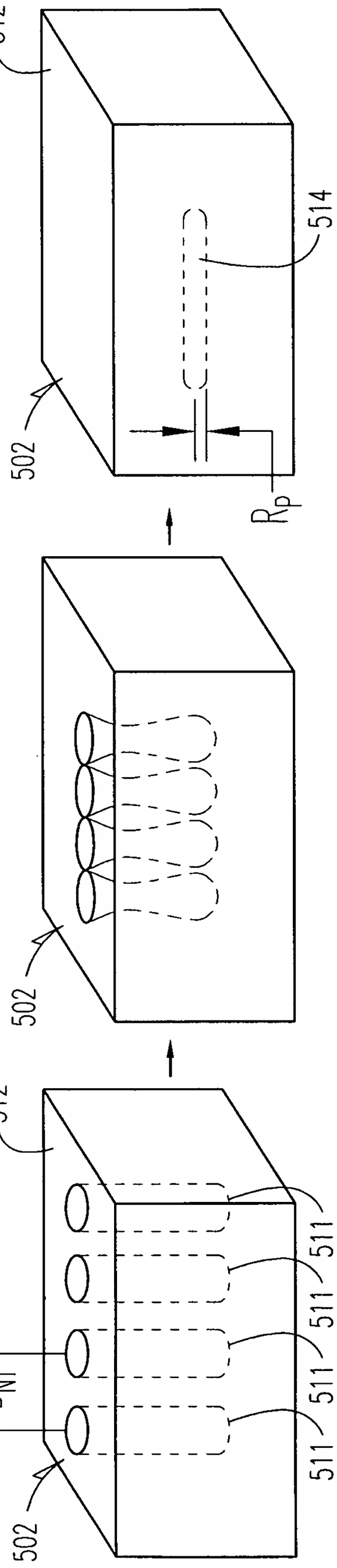

FIG. 5C FIG. 5B FIG. 5A

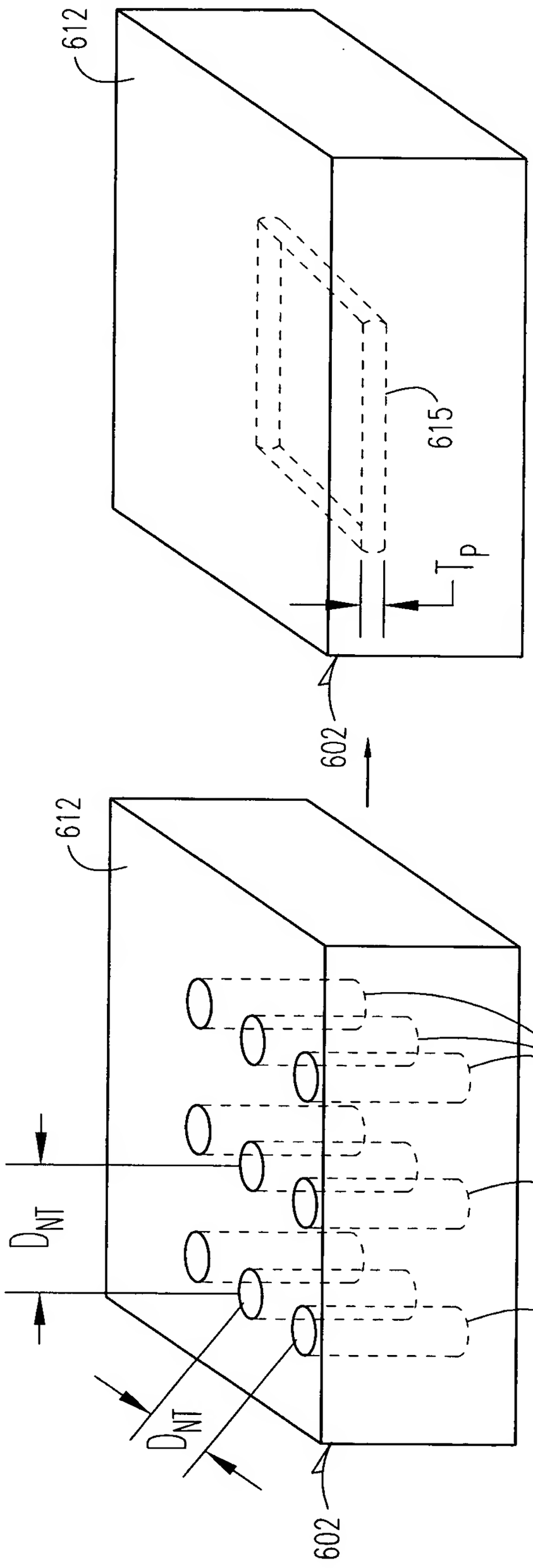

FIG. 6B

FIG. 6A

TITLE: GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.108US1

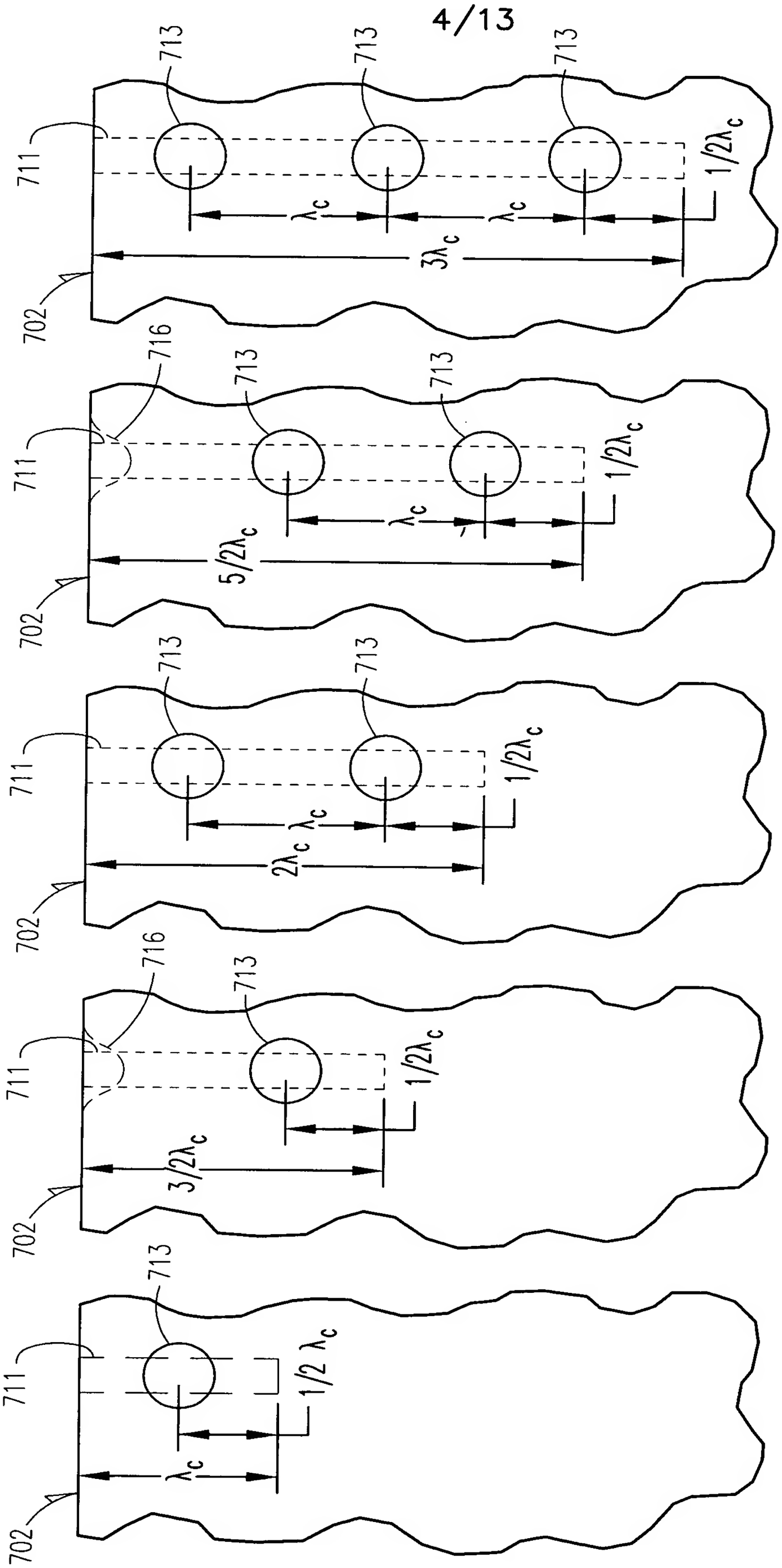

FIG. 7E

FIG. 7D

FIG. 7C

FIG. 7B

FIG. 7A

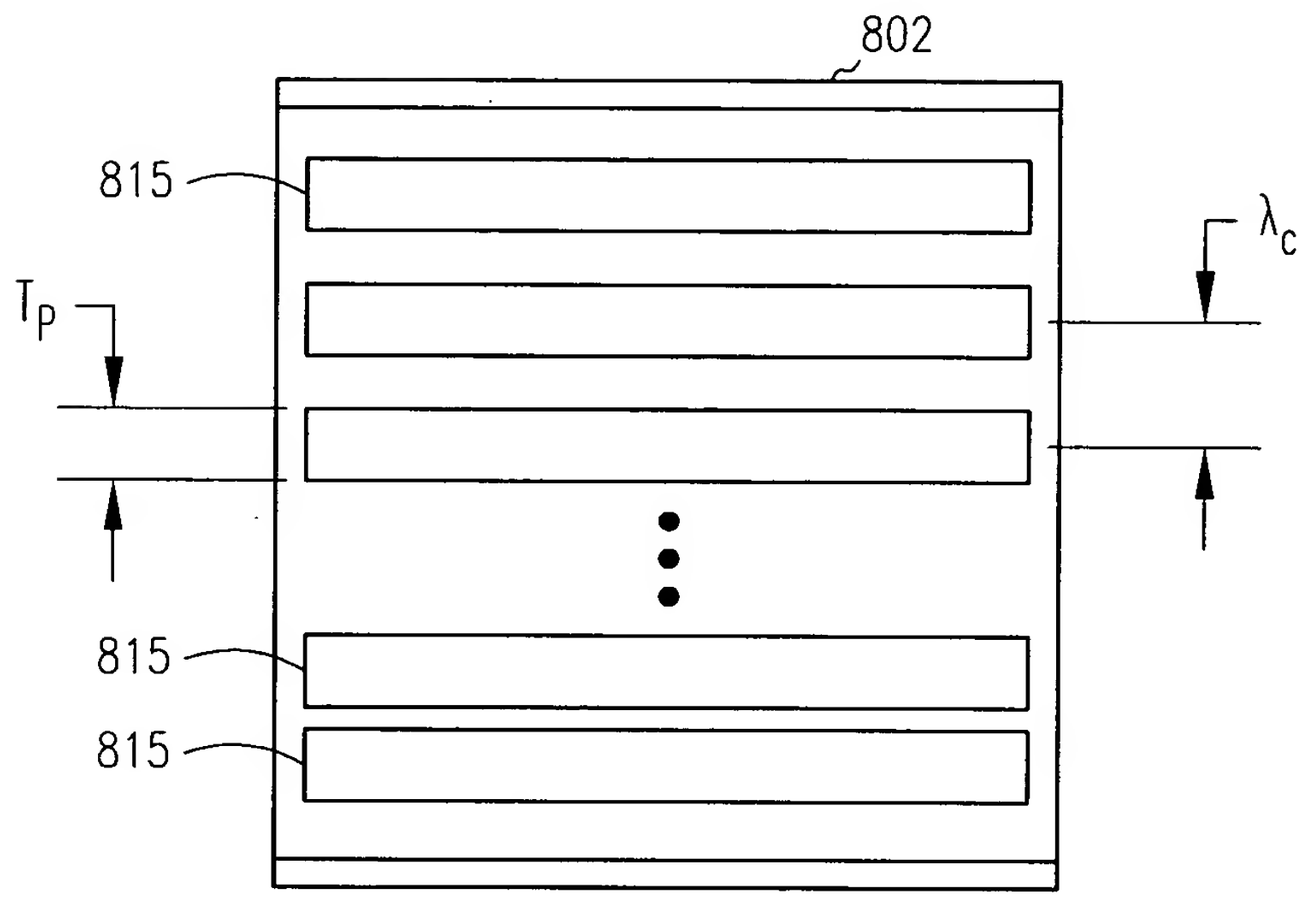

FIG. 8

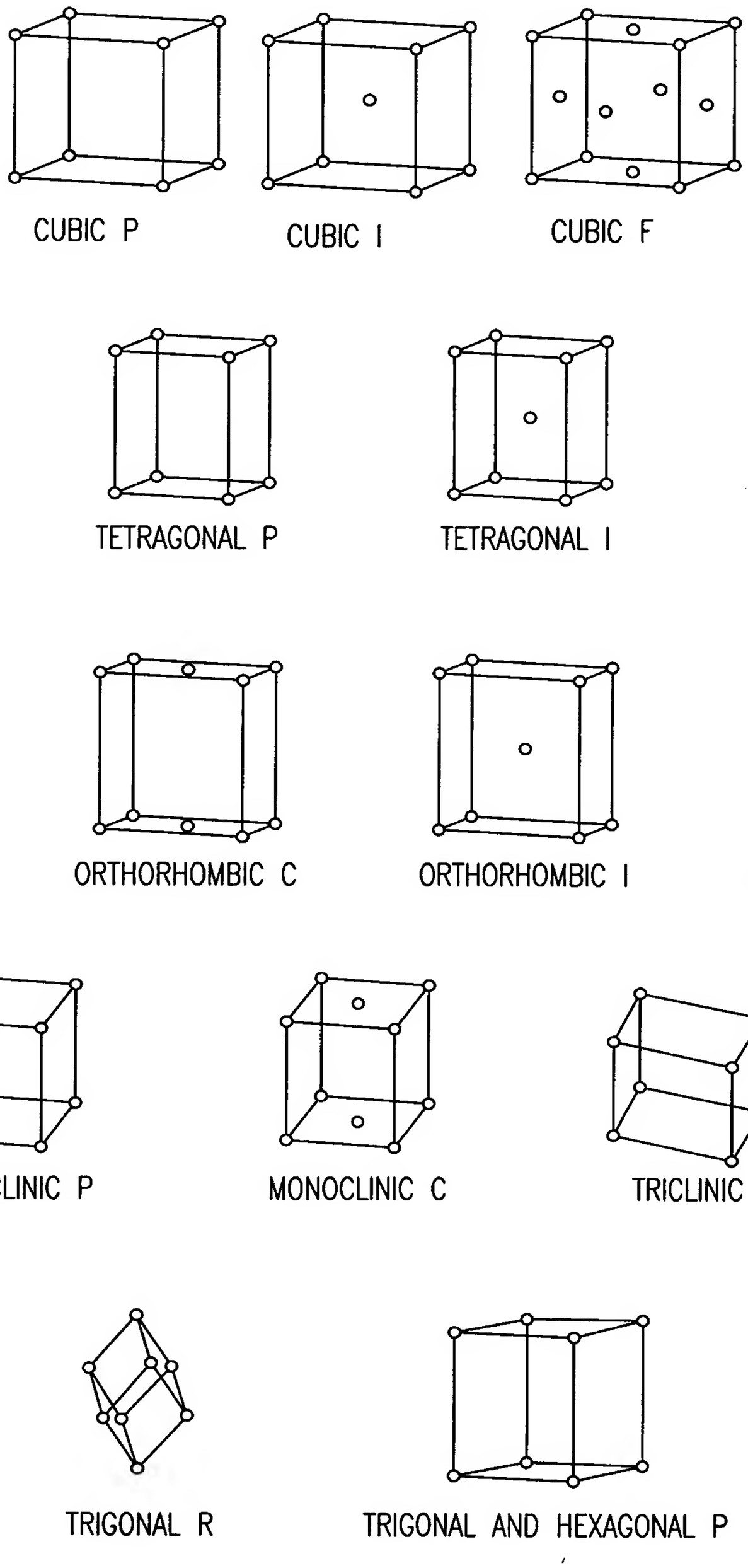
CUBIC P
CUBIC I
CUBIC F
TETRAGONAL P
TETRAGONAL I
ORTHORHOMBIC P
ORTHORHOMBIC C
ORTHORHOMBIC I
ORTHORHOMBIC F
MONOCLINIC P
MONOCLINIC C
TRICLINIC
TRIGONAL R
TRIGONAL AND HEXAGONAL P

FIG. 9

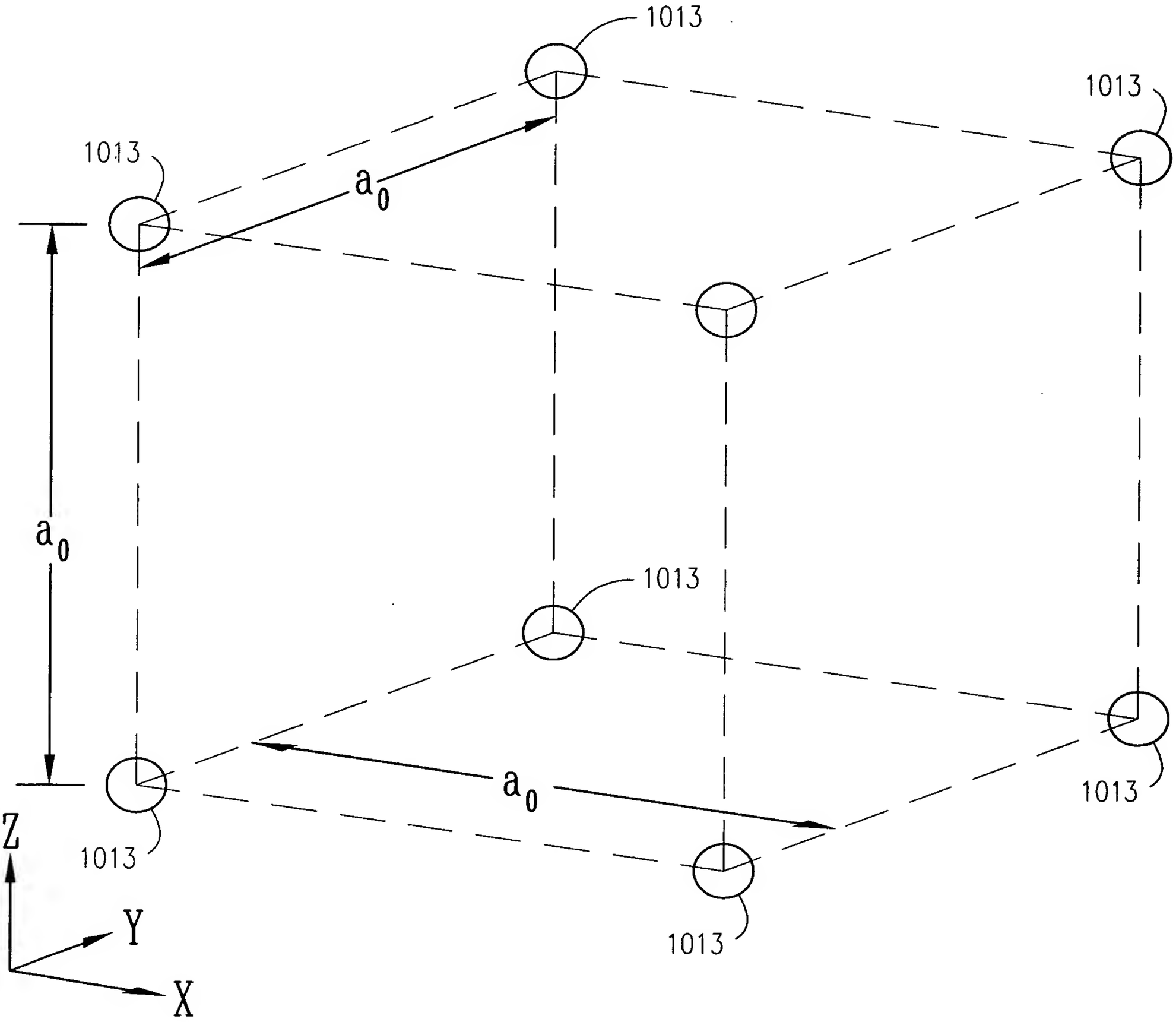

FIG. 10

TITLE: GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.108US1

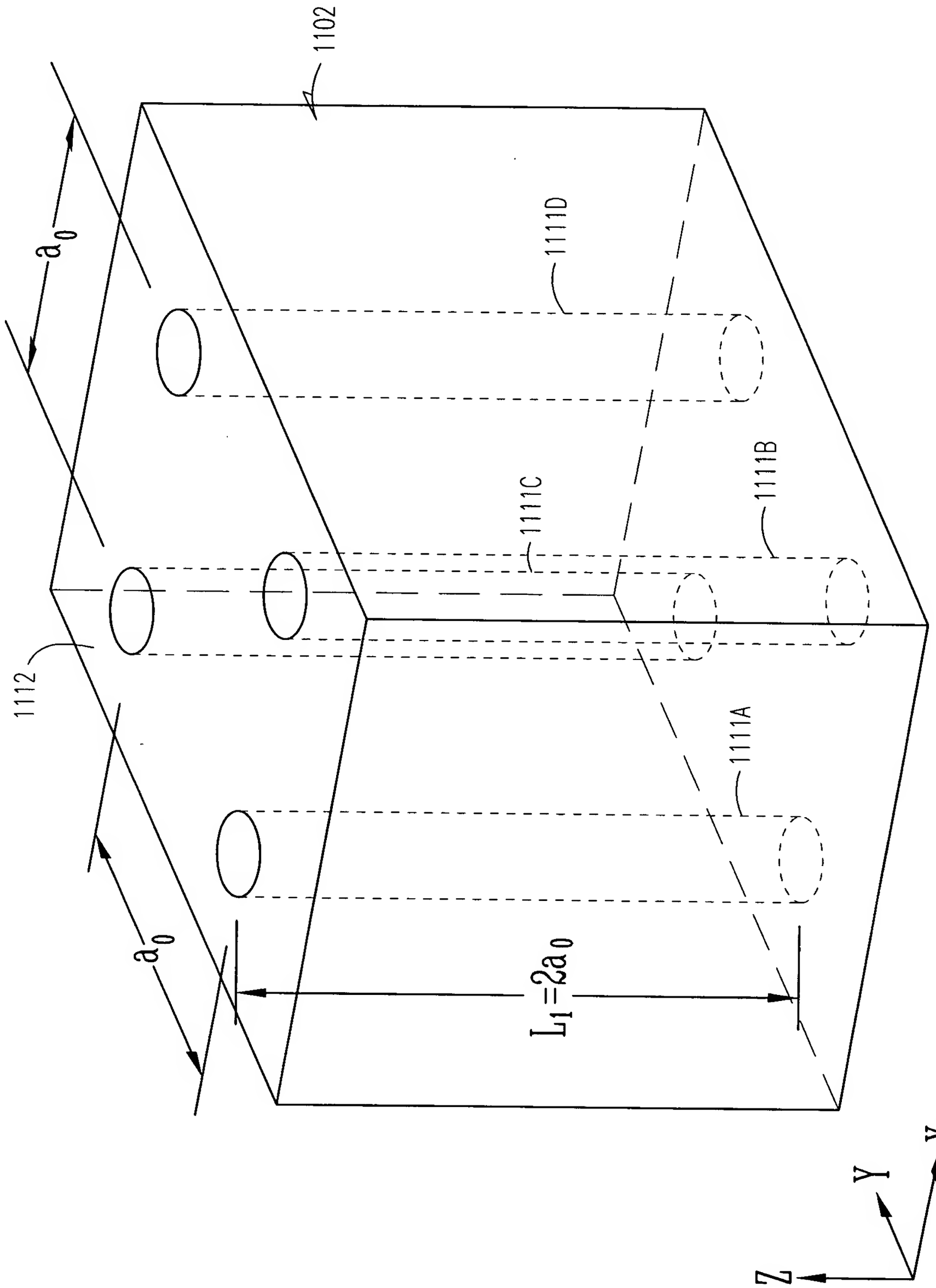

FIG. 11A

TITLE: GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.108US1

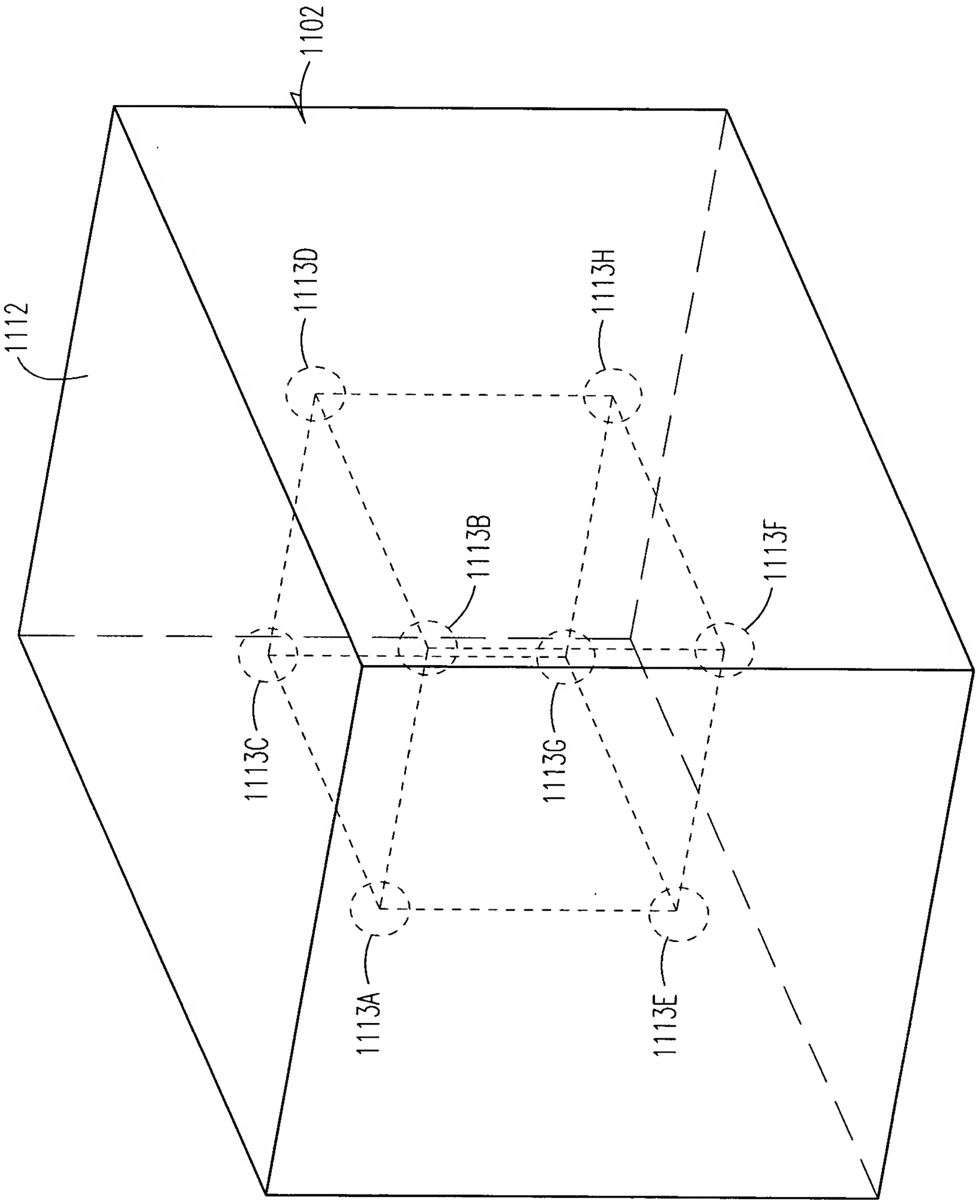

FIG. 11B

TITLE: GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
INVENTORS NAME: Leonard Forbes et al.
DOCKET NO.: 1303.108US1

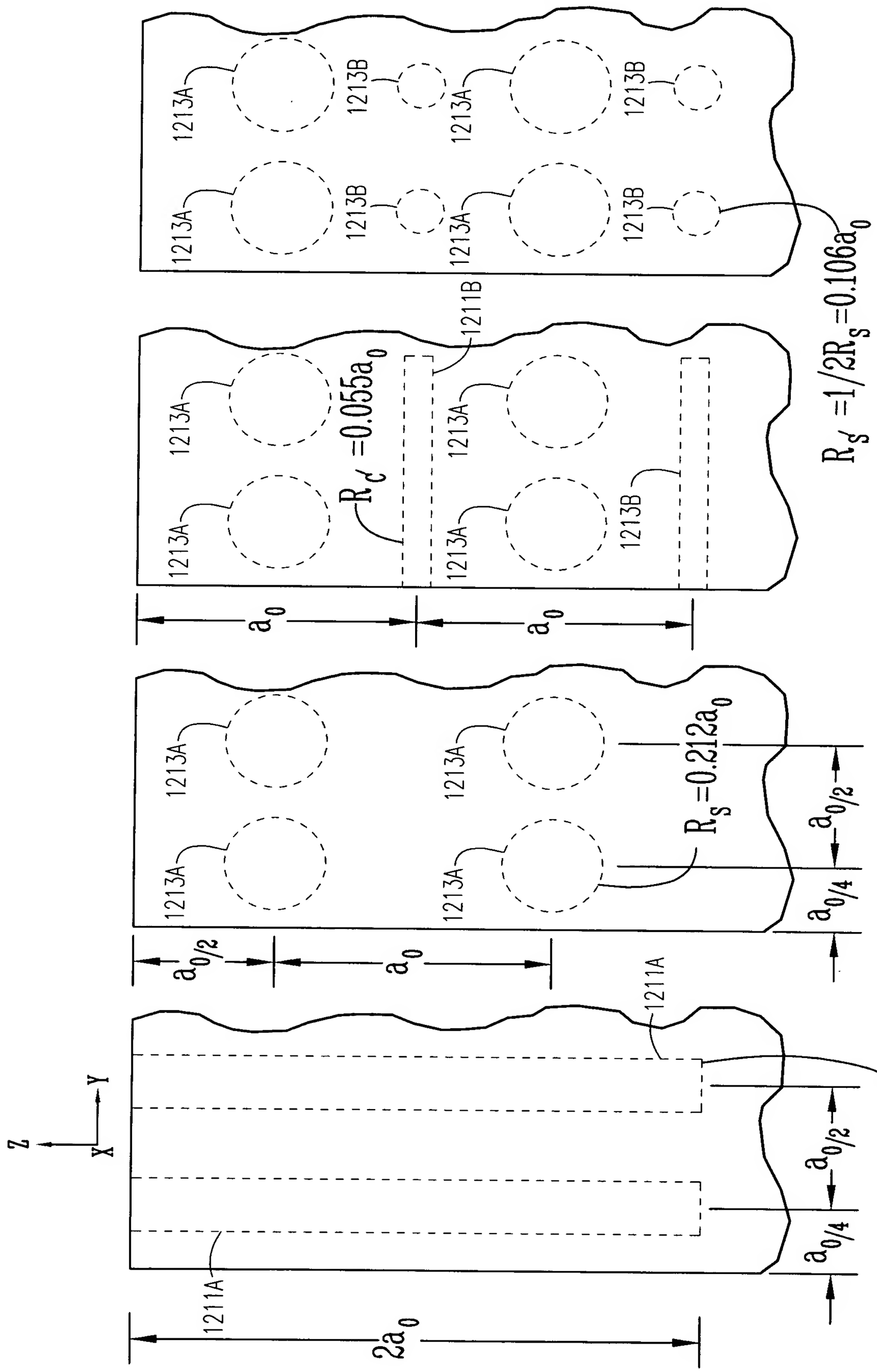

FIG. 12D

FIG. 12C

FIG. 12B

FIG. 12A

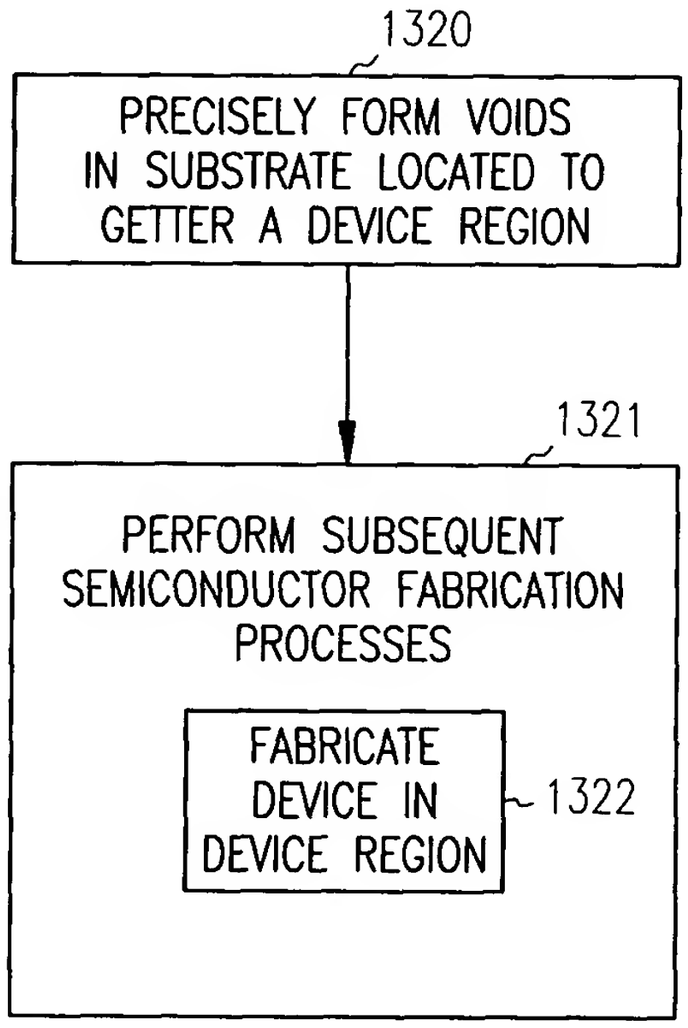
1320
PRECISELY FORM VOIDS IN SUBSTRATE LOCATED TO GETTER A DEVICE REGION
1321
PERFORM SUBSEQUENT SEMICONDUCTOR FABRICATION PROCESSES
FABRICATE DEVICE IN DEVICE REGION
1322

FIG. 13

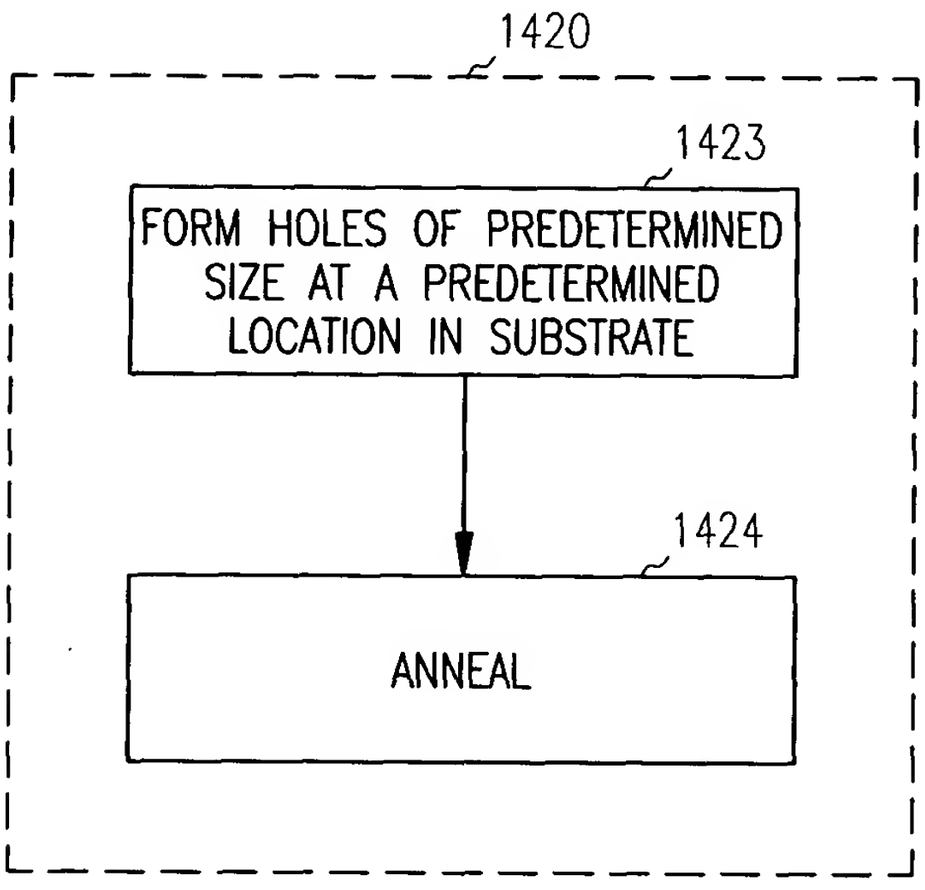
1420
1423
FORM HOLES OF PREDETERMINED SIZE AT A PREDETERMINED LOCATION IN SUBSTRATE
1424
ANNEAL

FIG. 14

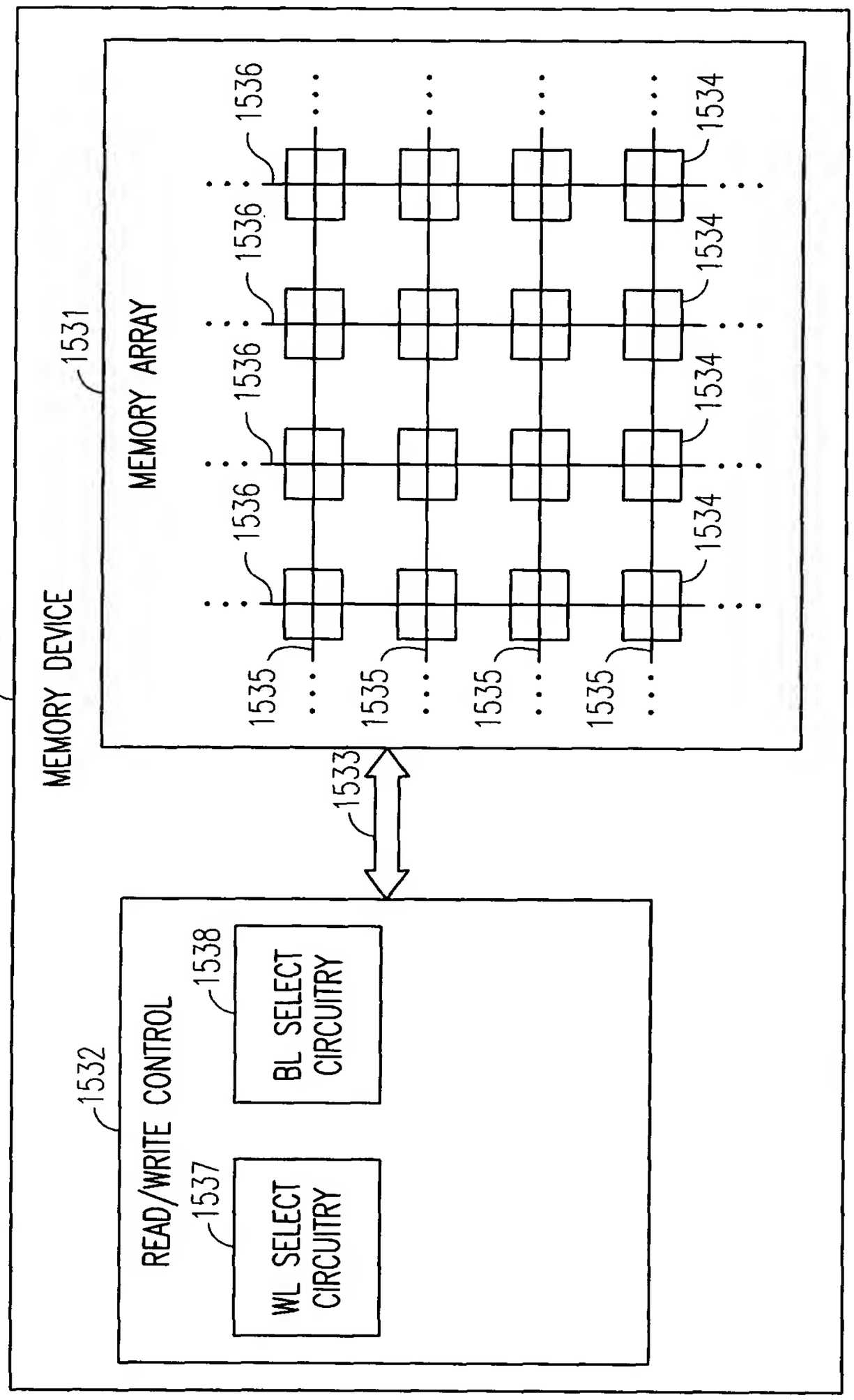
1530
MEMORY DEVICE
1531
MEMORY ARRAY
1536
1534
1535
1533
1532
READ/WRITE CONTROL
1538
BL SELECT CIRCUITRY
1537
WL SELECT CIRCUITRY

FIG. 15

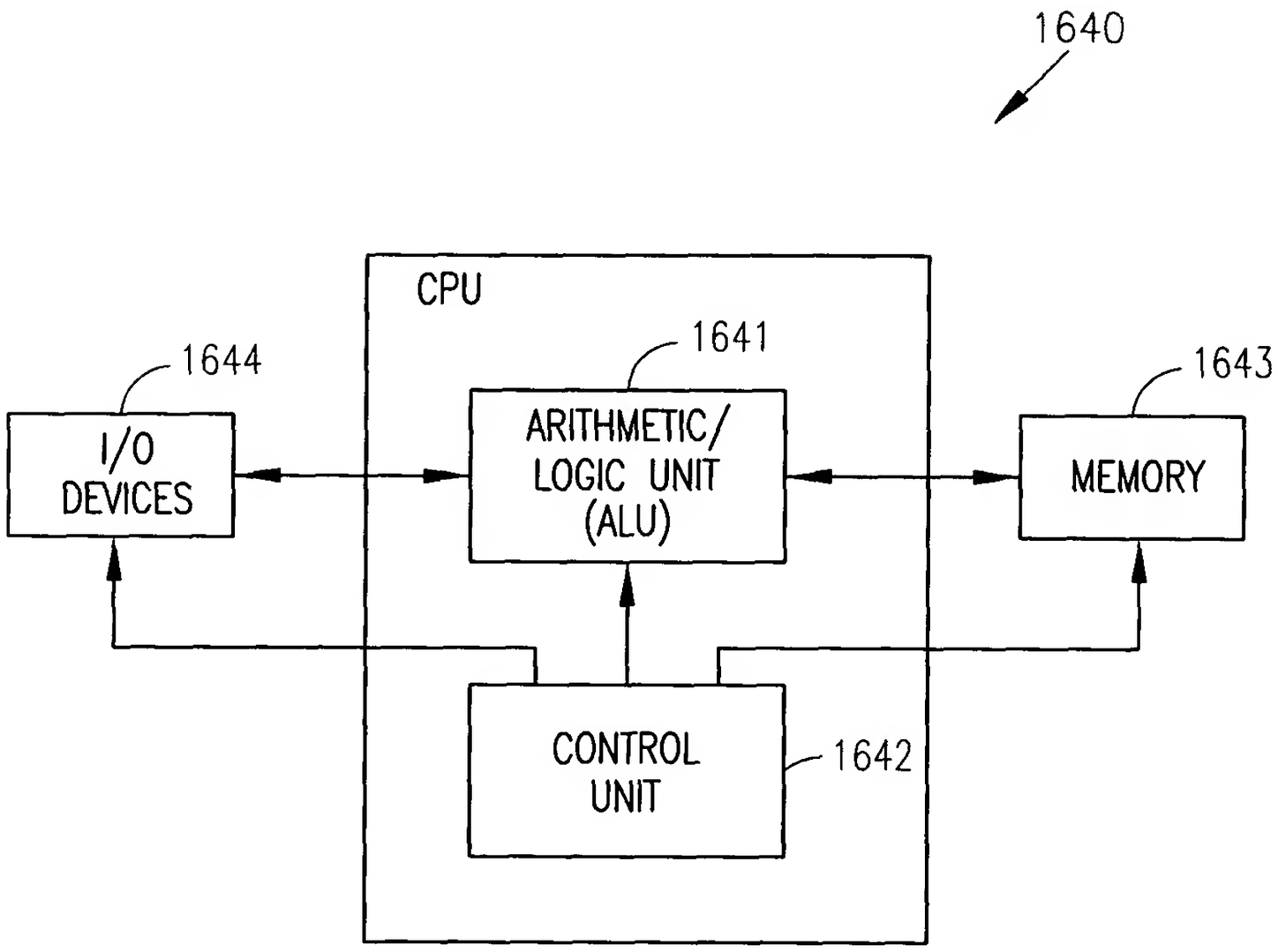
1640
CPU
1641
1644
1643
I/O DEVICES
ARITHMETIC/ LOGIC UNIT (ALU)
MEMORY
CONTROL UNIT
1642

FIG. 16